Design And Implementation Of A 6t Sram Cell For High-Speed And Low-Power Memory Applications

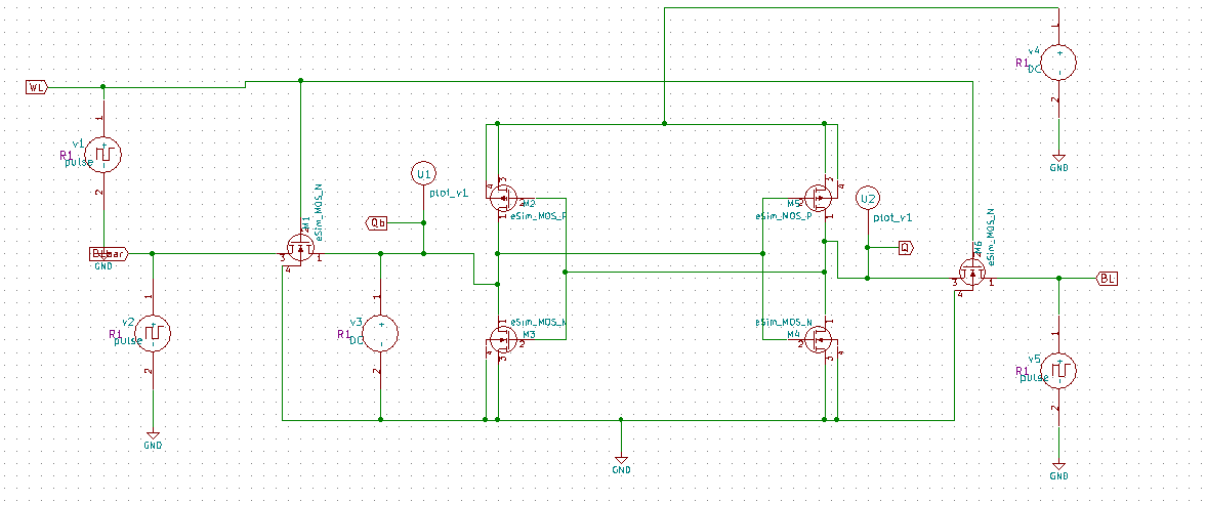
Introduction

The 6T SRAM (Six-Transistor Static Random Access Memory) cell is a core component in on-chip cache and high-speed memory architectures. It features two cross-coupled CMOS inverters, forming a bistable latch, and two access transistors. These access transistors, controlled by the word line (WL), connect the storage nodes to the bit lines (BL and BLB) during read and write operations.

This configuration allows the cell to stably store one bit of data ('0' or '1') without the need for periodic refreshing, unlike DRAM. The circuit's operation relies on coordinated control of the word line and bit lines. During a write operation, data is forced into the cell via the access transistors. Conversely, during a read operation, the stored value influences the voltage level on the bit lines.

This schematic illustrates a conventional 6T SRAM cell utilizing CMOS technology. NMOS transistors manage pull-down and access paths, while PMOS transistors serve as pull-ups in the cross-coupled inverters. This design delivers fast access, low power consumption, and robust data retention, making it ideal for high-density memory arrays and low-power embedded systems.

Circuit Diagram



Outputs

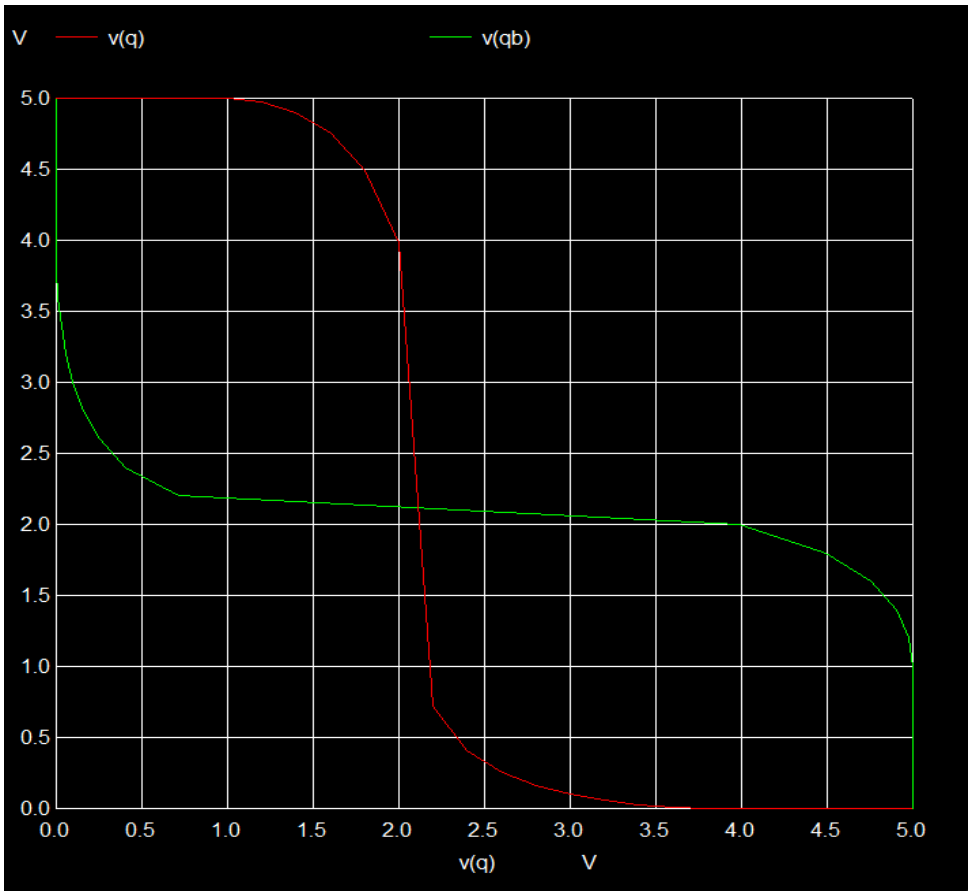


Fig.1-DC transfer characteristic (the classic *butterfly curve*) used for SRAM cell Static Noise Margin (SNM) analysis

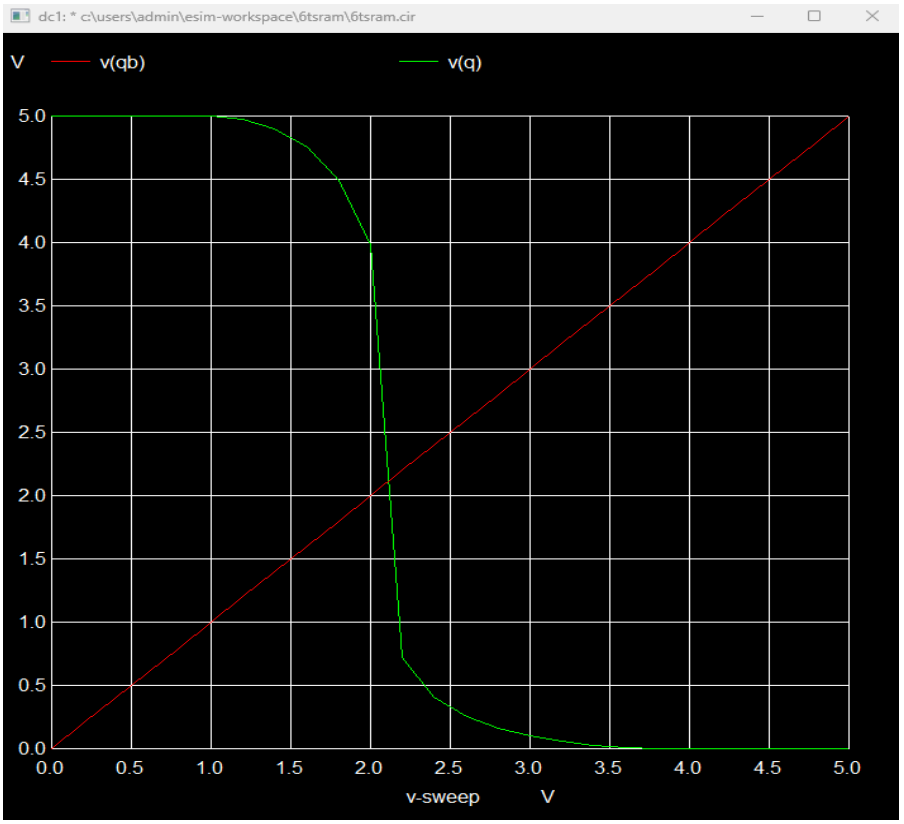


Fig.2 VTC characteristics of Basic Inverter(included in SRAM)

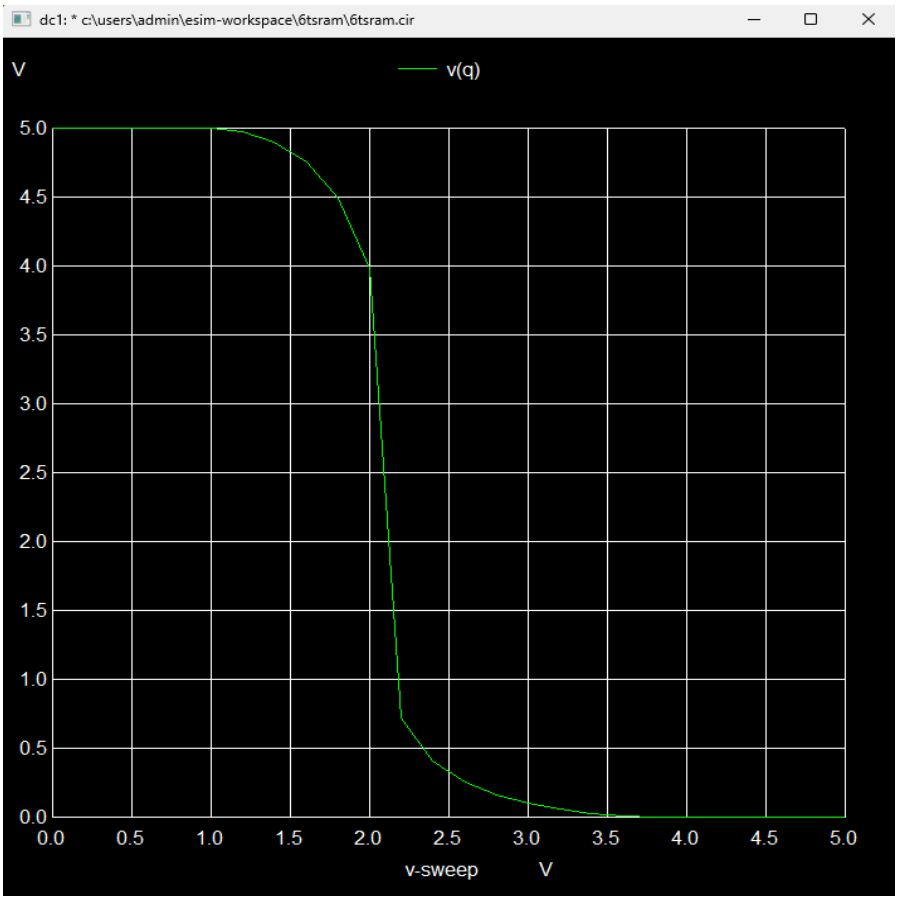


Fig.4 Output of INV1

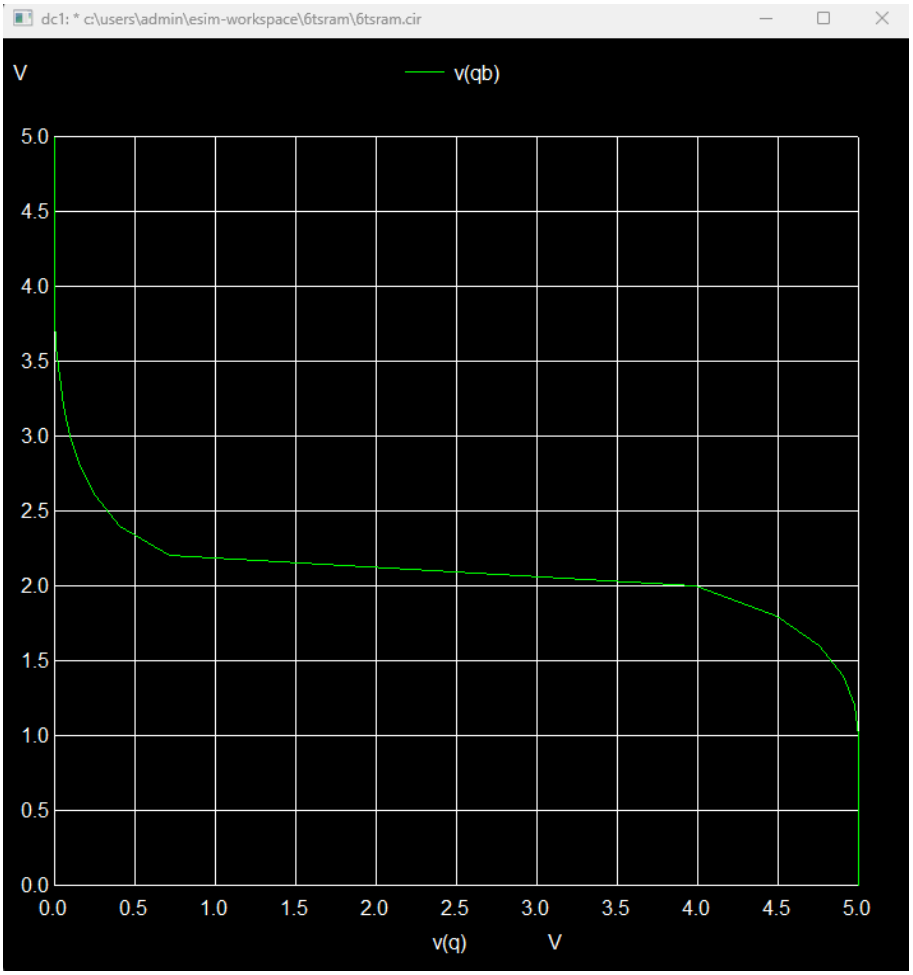


Fig.5 Output of INV1

Conclusion

The DC analysis of the 6T SRAM cell, the obtained butterfly curve clearly demonstrates the bistable operation of the cross-coupled inverters, confirming the cell's ability to hold two stable logic states. The symmetry of the Q and Qb voltage transfer characteristics indicates proper transistor sizing and stable operation at the given supply voltage. The Static Noise Margin (SNM) can be extracted from this curve, validating the cell's robustness against noise and process variations. Overall, the simulation results verify the correct functioning and reliable data retention capability of the designed 6T SRAM cell.

References

P. T, R. L. Paulraj, S. Kulkarni, T. A. Kumbhare, N. M and D. M. M, "6T SRAM: A Technical Overview," 2023 International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS), Bangalore, India, 2023, pp. 698-702, doi: 10.1109/ICAECIS58353.2023.10170407. keywords: {Temperature;Simulation;Electronics industry;Stability criteria;Random access memory;Voltage;Very large scale integration;Memory cell;Design complexity;EDA Power;Area;Speed},

Shukla, Neeraj & Birla, Shilpi & Singh, R K & Pattanaik, Manisha. (2011). Speed and Leakage Power Trade-off in Various SRAM Circuits. International Journal of Computer and Electrical Engineering. 244-249. 10.7763/IJCEE.2011.V3.321.

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