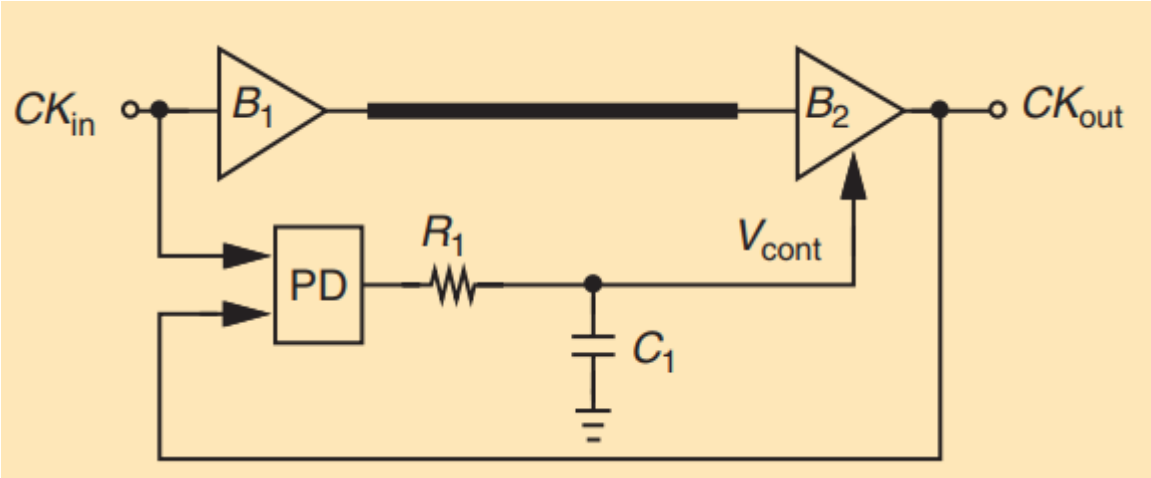
Voltage Controlled Delay Line For DLL

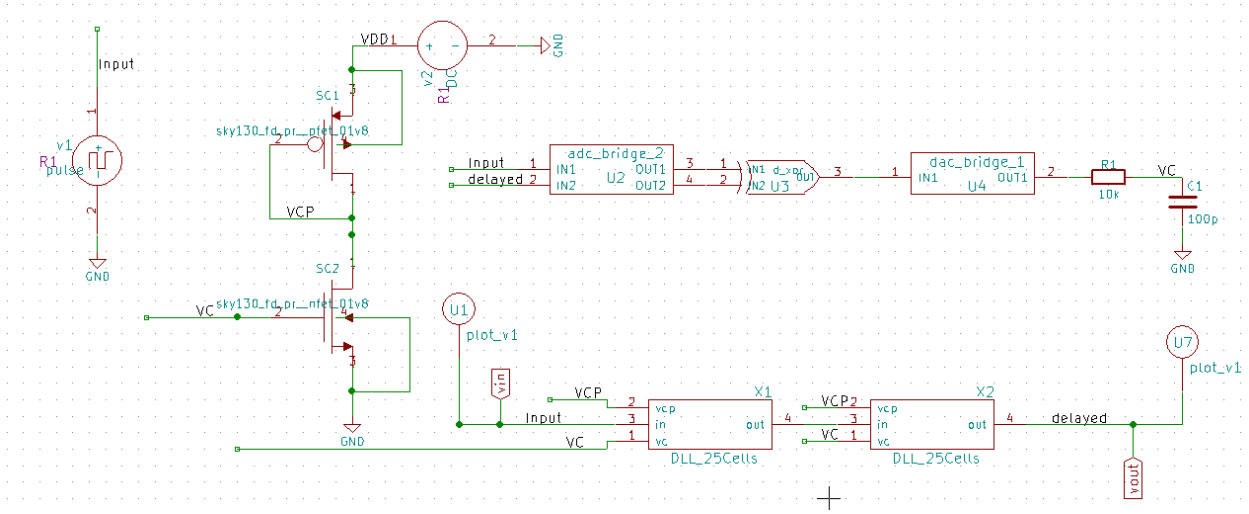
Simulated on eSim from FOSSE

Introduction

Delay-locked loops (DLLs) can be considered as feedback circuits that phase lock an output to an input without the use of an oscillator. In some applications, DLLs are necessary or preferable over phase-locked loops (PLLs), with their advantages including lower sensitivity to supply noise and lower phase noise. This article deals with fundamental DLL design concepts.



Description



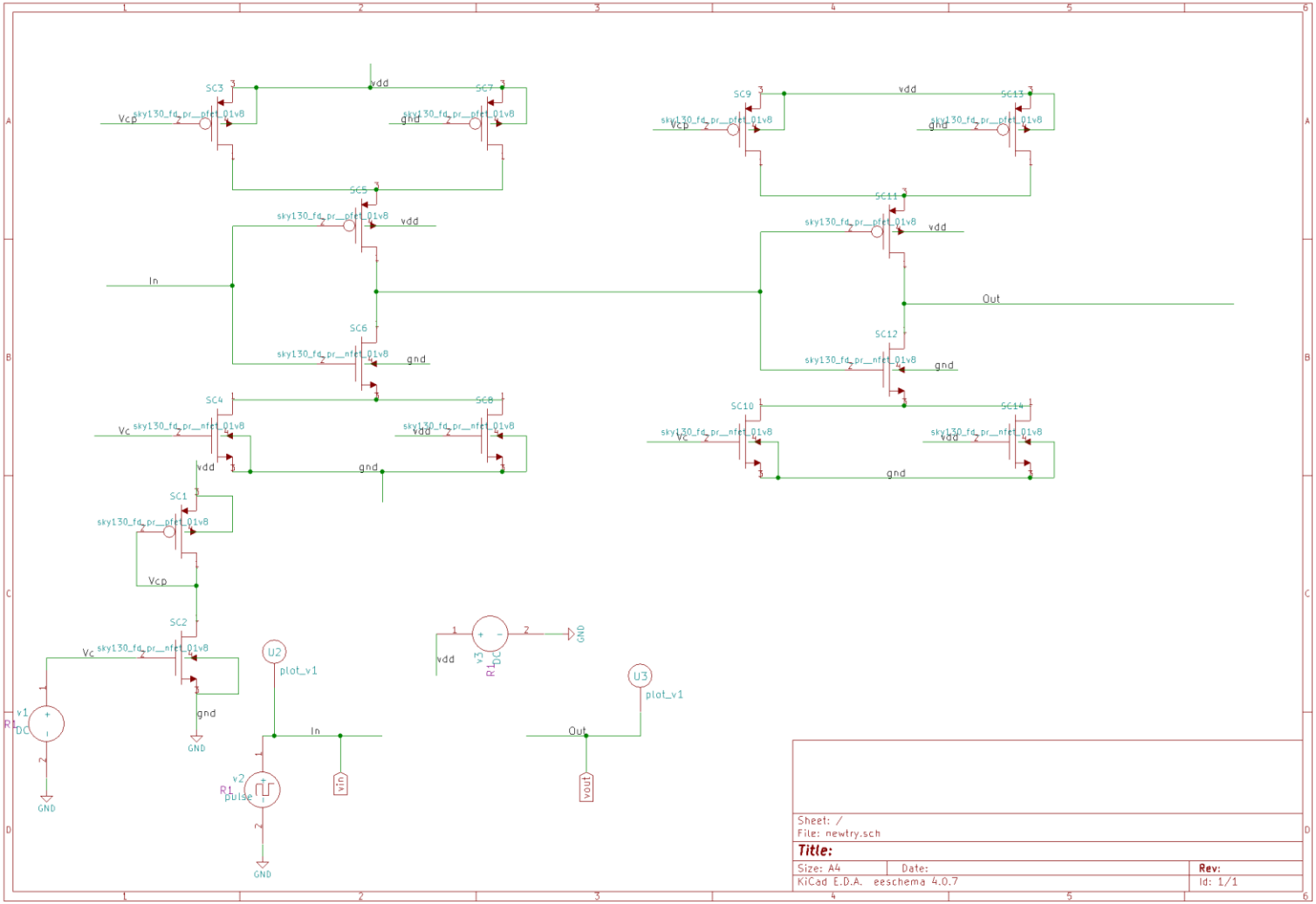
Final DLL Circuit Schematic

Throughout this paper we are simulating a pre-designed Voltage Controlled Delay Line(VCDL) on **eSim**. The figure above shows the final schematic of the VCDL test bench, which is mainly a simple topology of the DLL using simple Phase Detector (PD) which is the XOR gate between ADC/DAC modules to match the simulation requirements. The basic delay line is made out of simple inverters of the same sizing, each two of them compose a buffer which is the main single cell of the line.

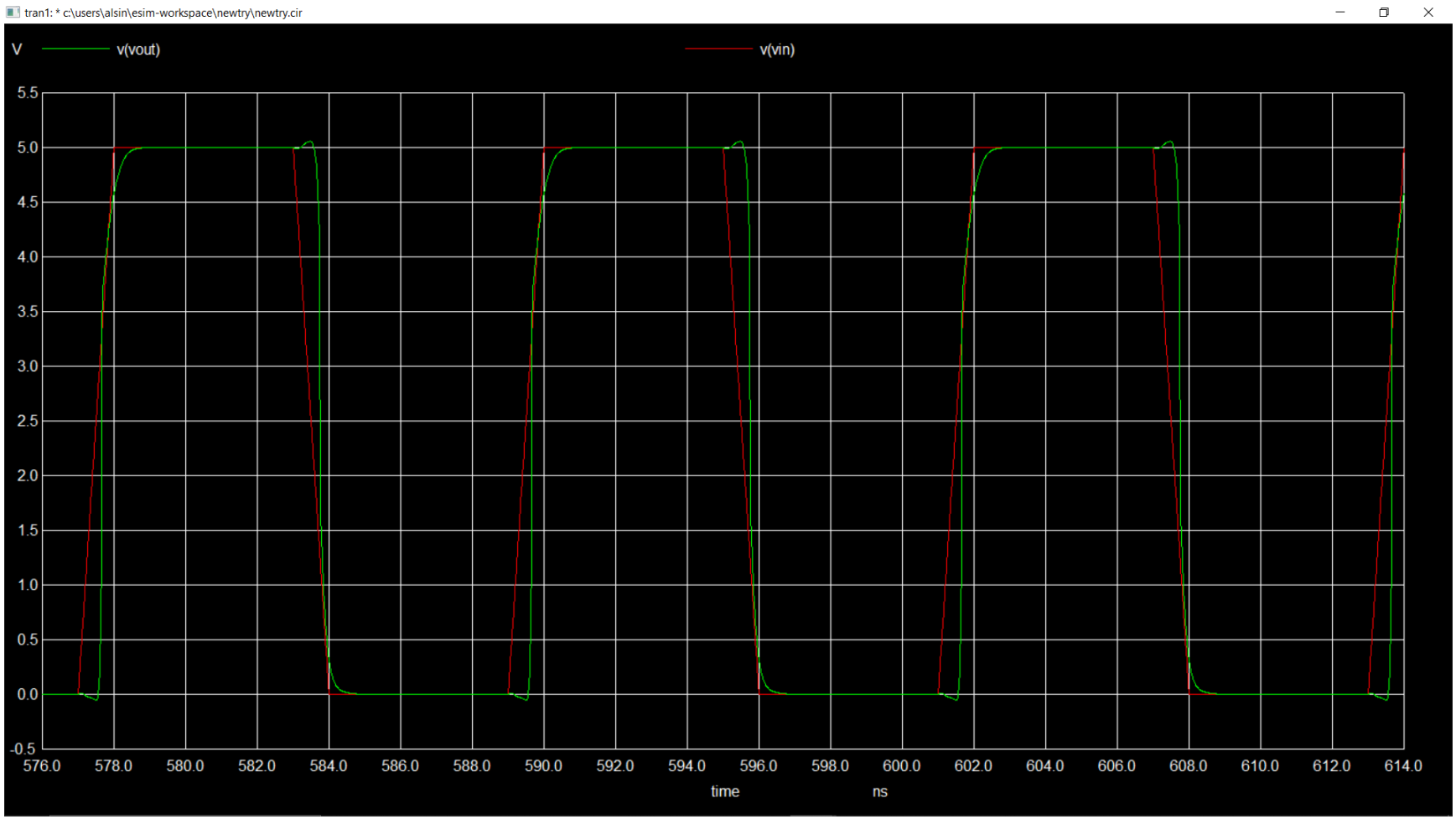
The current mirror connection at the left -two transistors- to generate the Pull Up Network(PUN) control voltage (Vcp) in contrast to the PDN which gets Vc out of the LPF smoothing circuit (R+C).

Following are the complete details of the design and simulations.

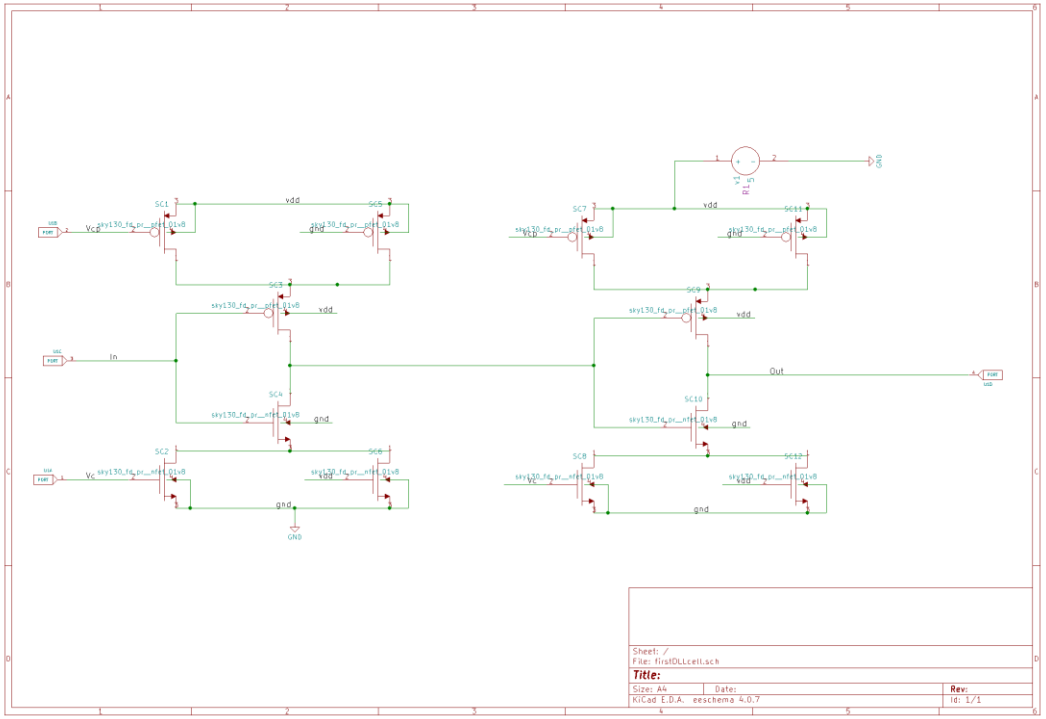
The VCDL is composed of 50 distributed over 2 DLL_25Cells, which results in transistor count of T = Cells * Transistors/Cell = 50 * 12 = 600 Transistors

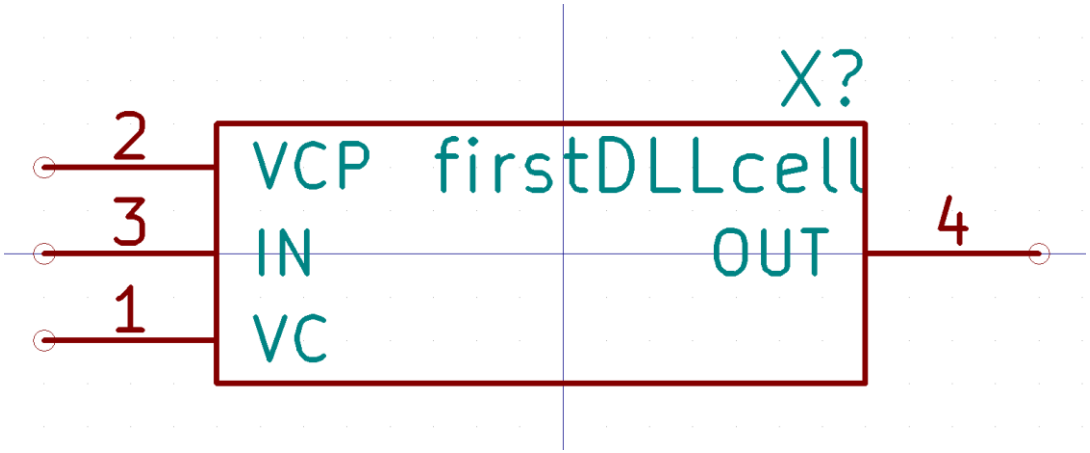


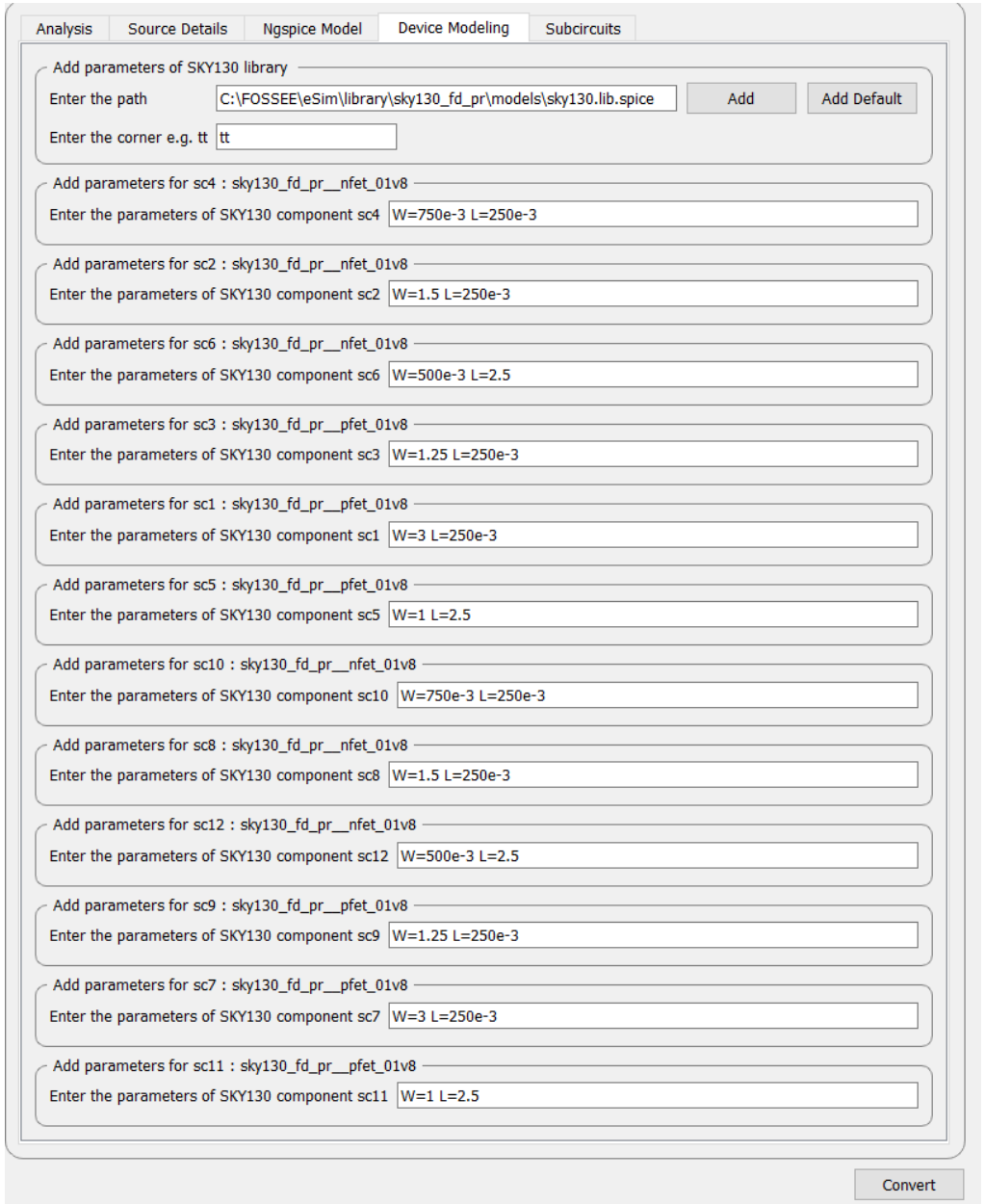
1 Cell Test Bench

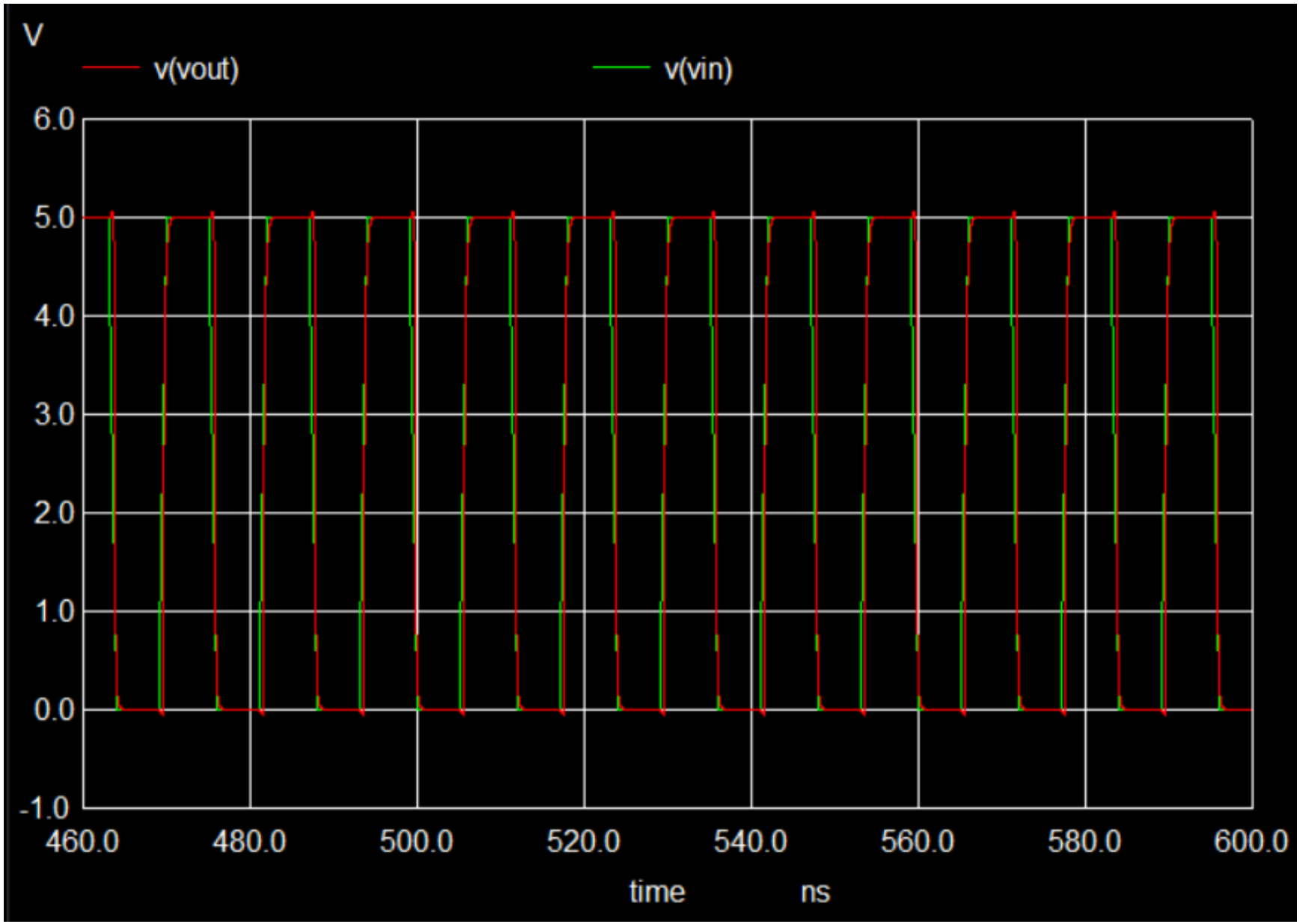


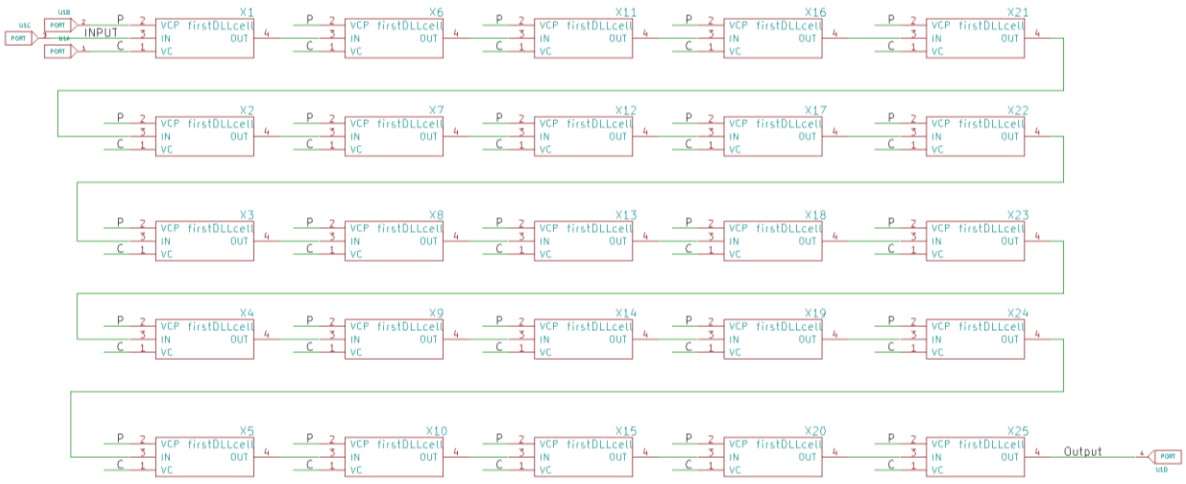
1 cell simulation results


vdd
gnd
In
Out
Vc
Vcp
GND
Sheet: /
File: firstDLLcell.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema 4.0.7
Id: 1/1

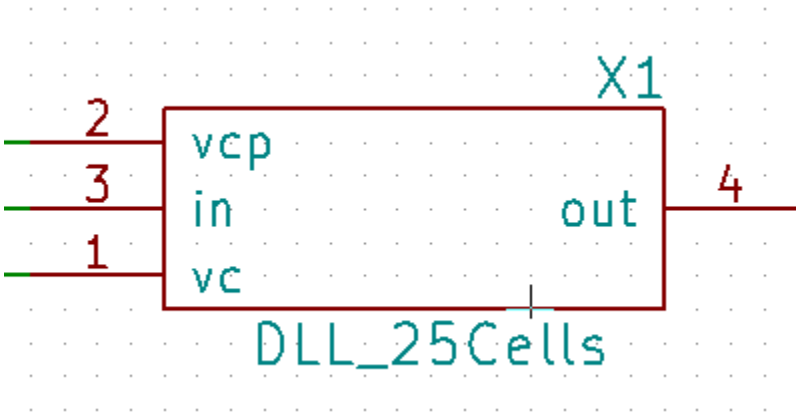

X?
2
3
1
VCP
IN
VC
firstDLLcell
OUT
4


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters of SKY130 library
Enter the path
C:\FOSSEE\eSim\library\sky130_fd_pr\models\sky130.lib.spice
Add
Add Default
Enter the corner e.g. tt
tt
Add parameters for sc4 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc4
W=750e-3 L=250e-3
Add parameters for sc2 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc2
W=1.5 L=250e-3
Add parameters for sc6 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc6
W=500e-3 L=2.5
Add parameters for sc3 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc3
W=1.25 L=250e-3
Add parameters for sc1 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc1
W=3 L=250e-3
Add parameters for sc5 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc5
W=1 L=2.5
Add parameters for sc10 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc10
W=750e-3 L=250e-3
Add parameters for sc8 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc8
W=1.5 L=250e-3
Add parameters for sc12 : sky130_fd_pr__nfet_01v8
Enter the parameters of SKY130 component sc12
W=500e-3 L=2.5
Add parameters for sc9 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc9
W=1.25 L=250e-3
Add parameters for sc7 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc7
W=3 L=250e-3
Add parameters for sc11 : sky130_fd_pr__pfet_01v8
Enter the parameters of SKY130 component sc11
W=1 L=2.5
Convert

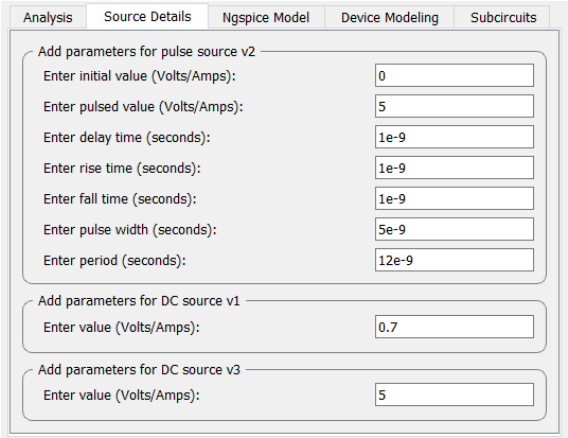

V
v(vout)
v(vin)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
460.0
480.0
500.0
520.0
540.0
560.0
580.0
600.0
time
ns



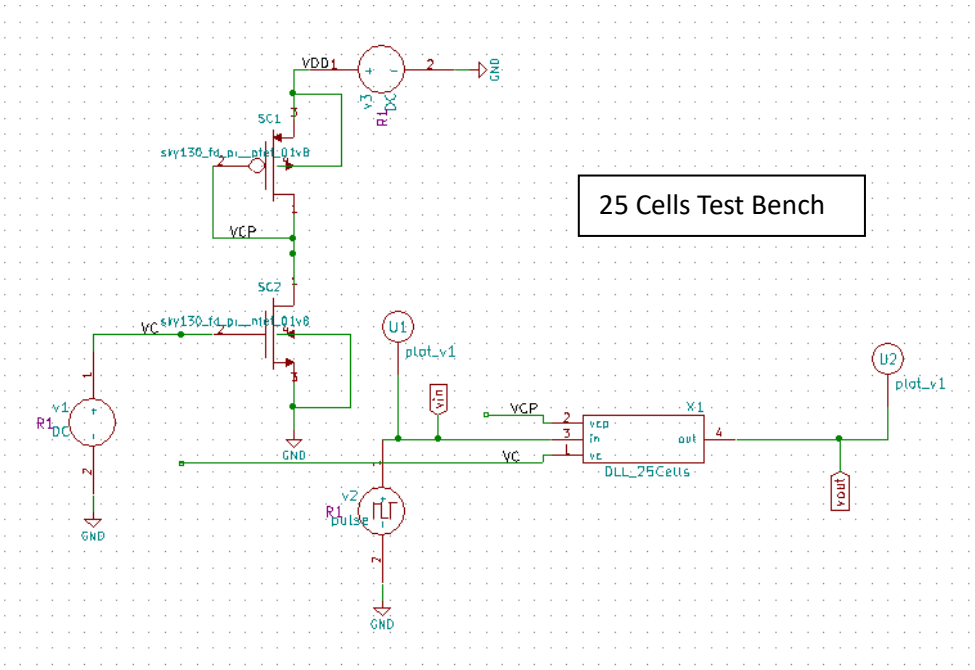
25 Cells schematic (25*[firstDLLcell](#))

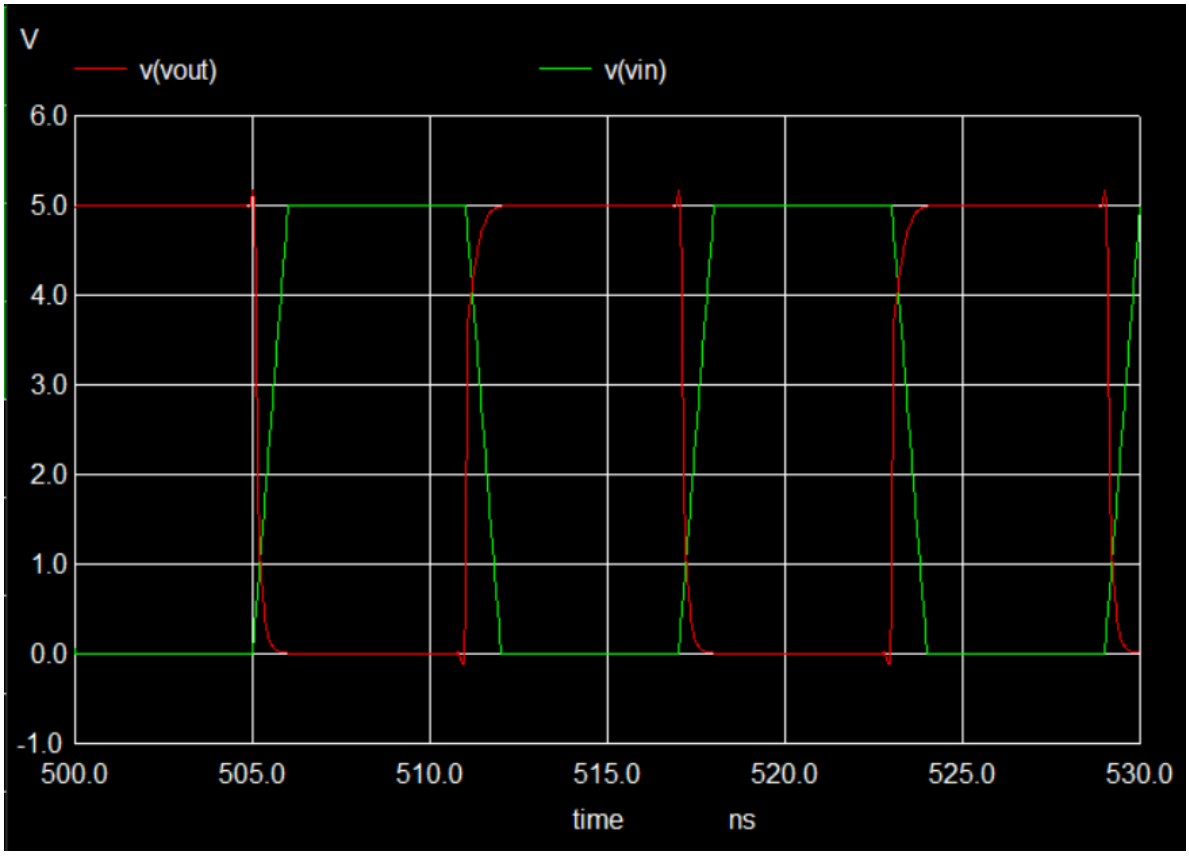


25 cells symbol

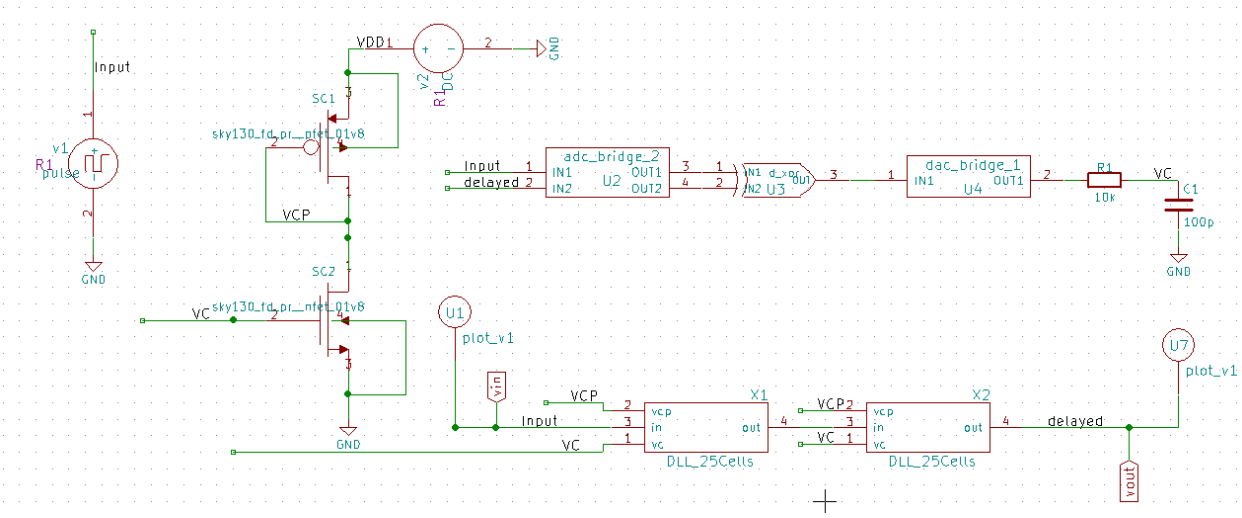


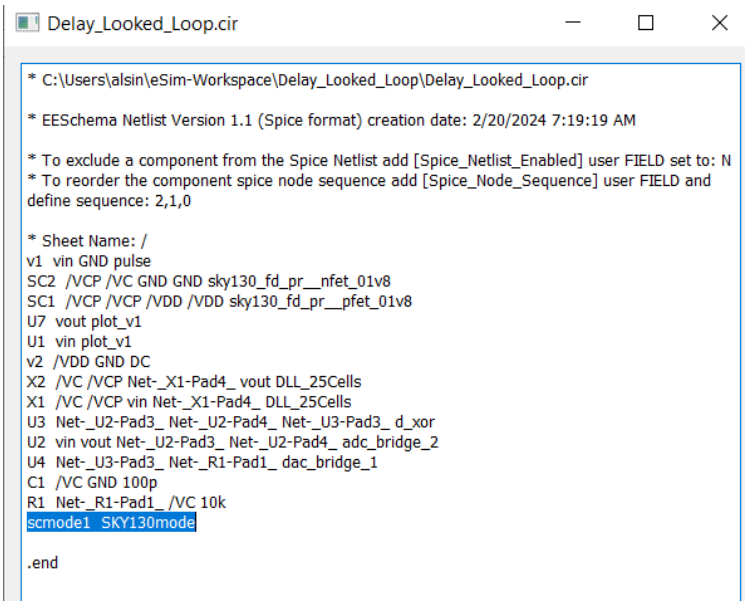
Simulation Setup



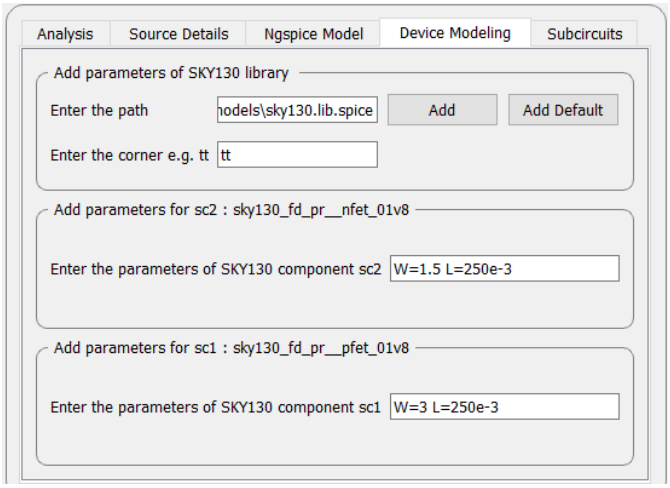


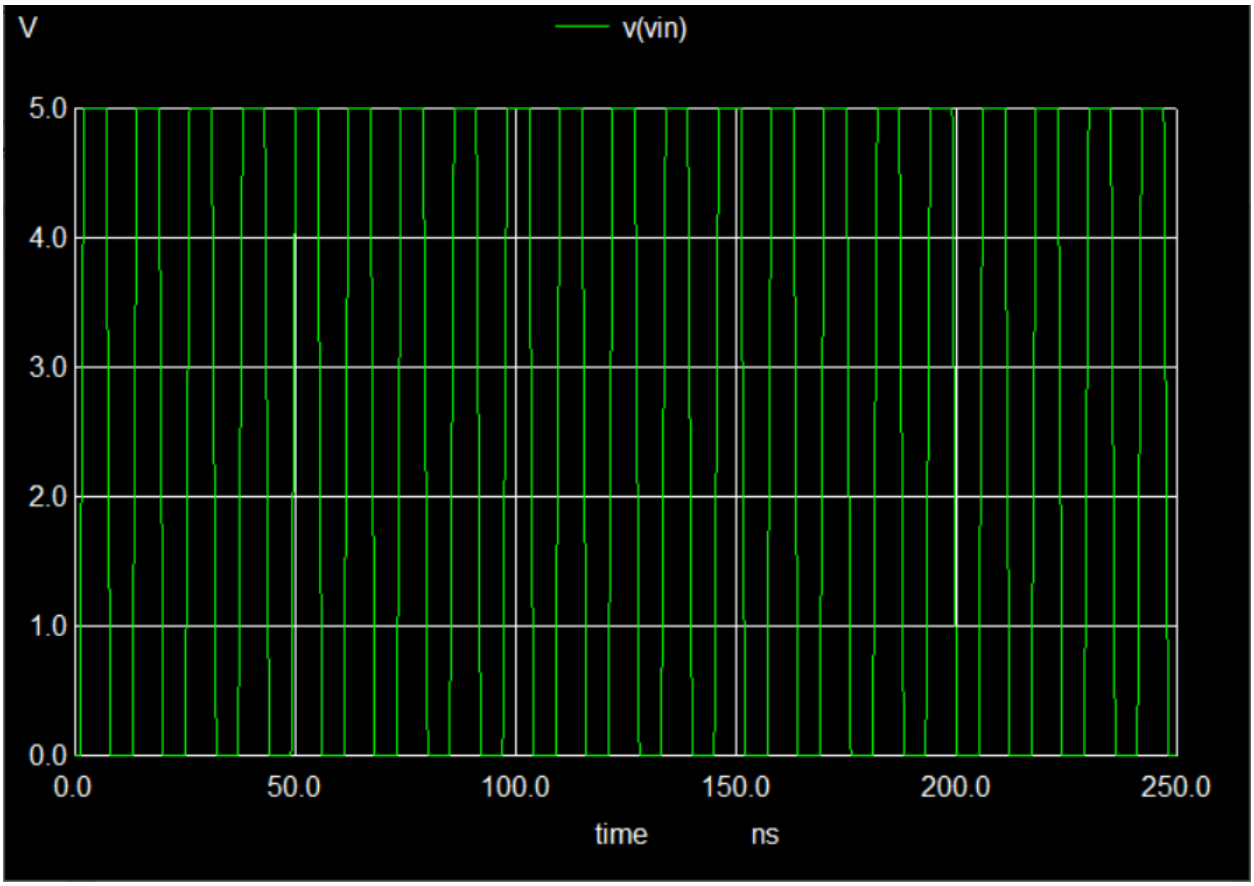
25 Cells Simulation Output

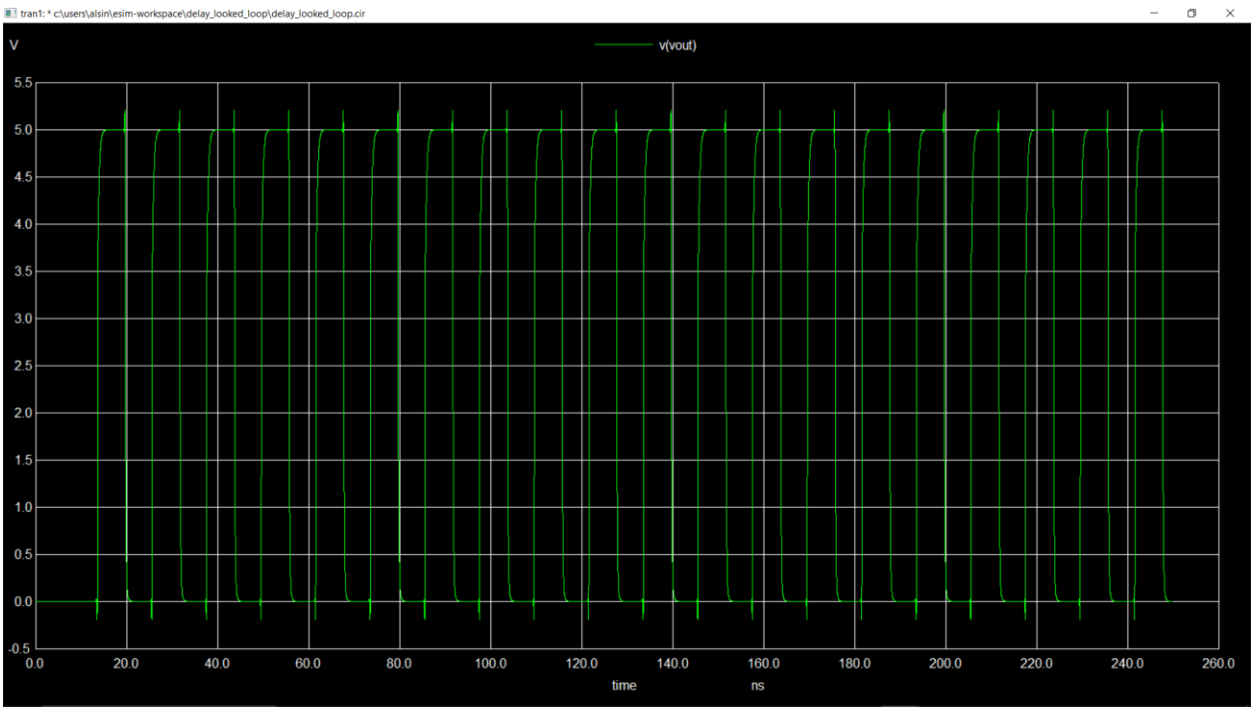




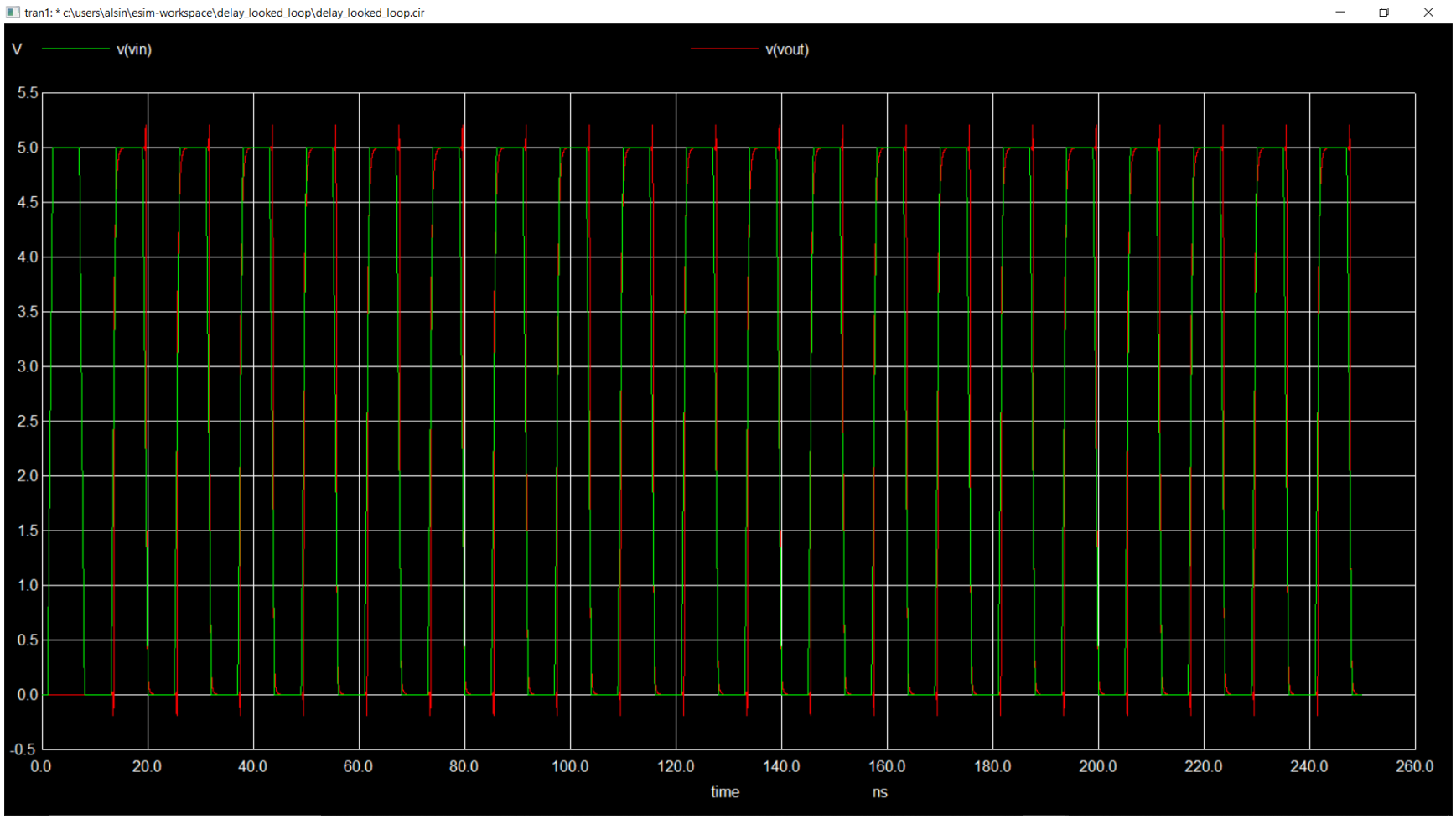
Don’t forget to include the highlighted line



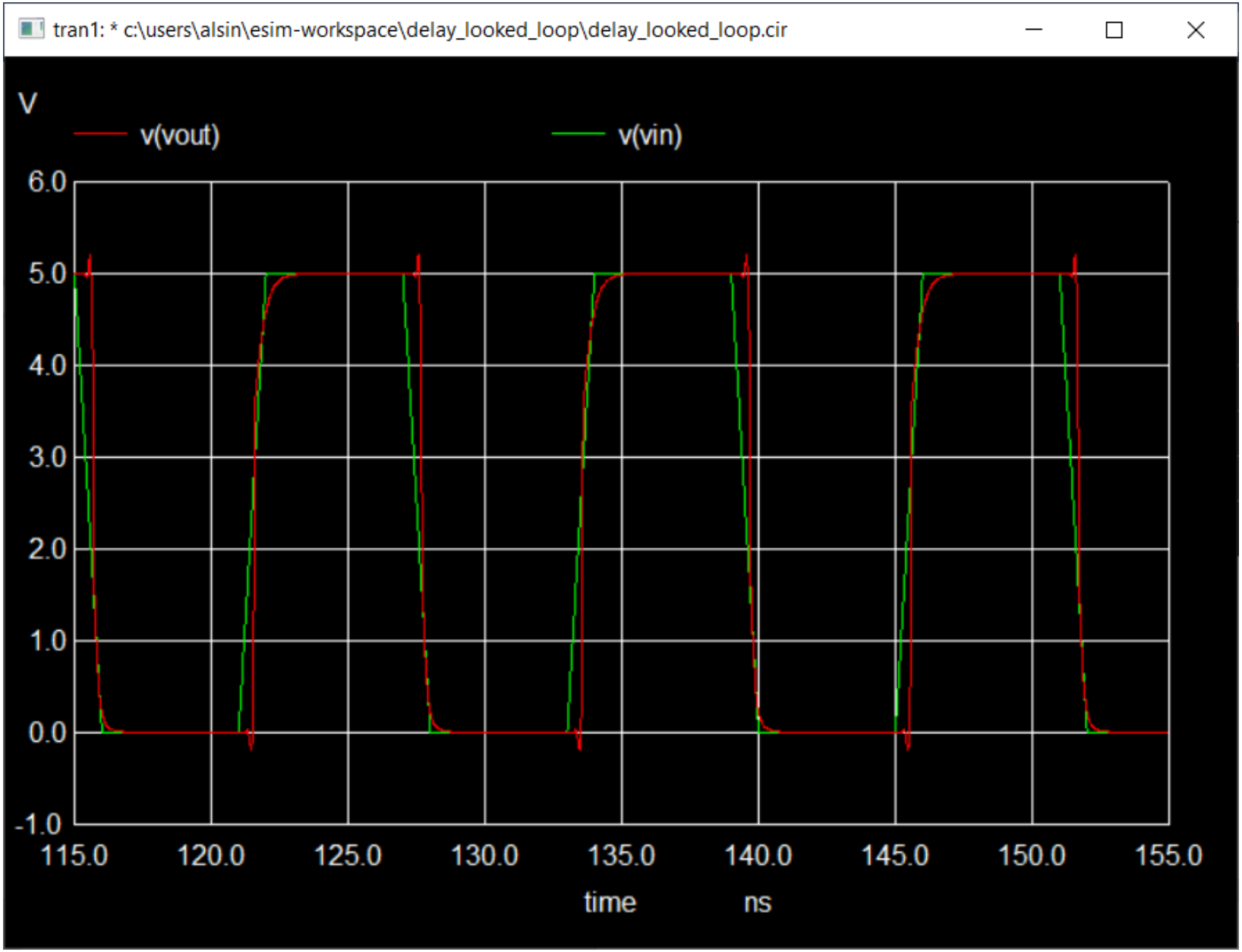


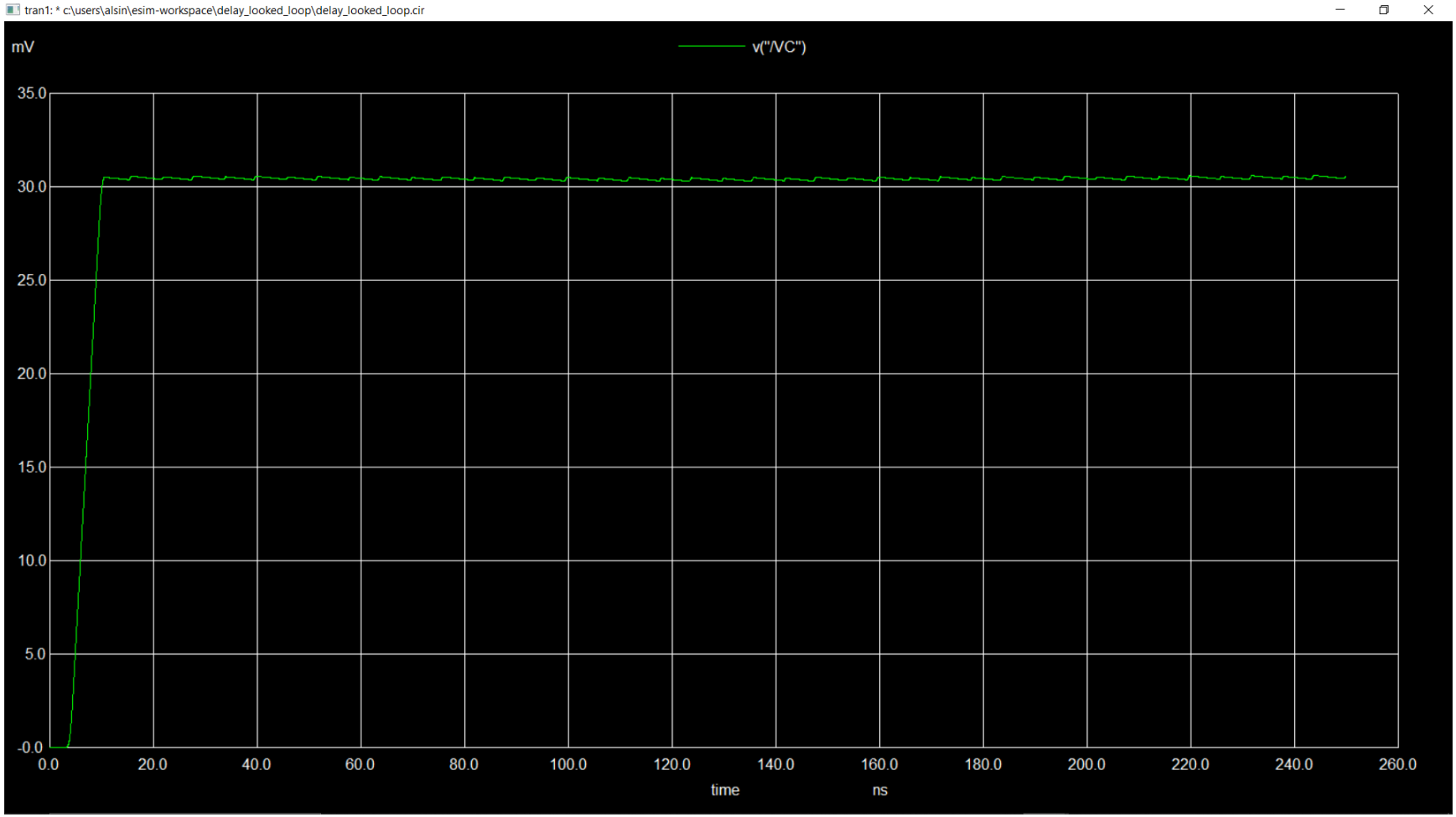


Around 13ns delay at the output

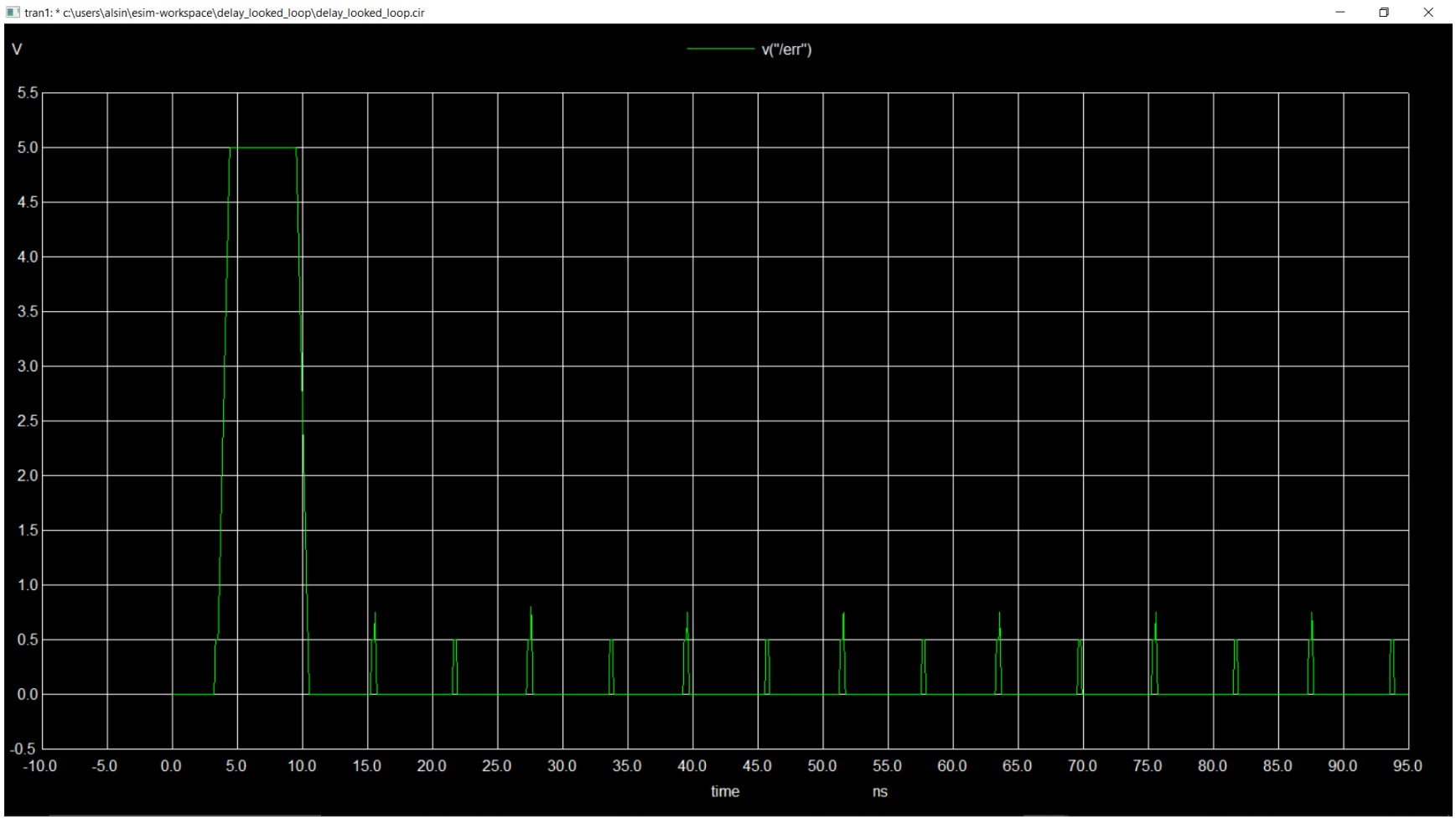


IN/Out overlaid


tran1: * c:\users\alsin\esim-workspace\delay_looked_loop\delay_looked_loop.cir
V
v(vout)
v(vin)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
115.0
120.0
125.0
130.0
135.0
140.0
145.0
150.0
155.0
time
ns



Delay Line Control Voltage (VC) change with time



Error signal (after XOR)

References:

- B. Razavi, "The Delay-Locked Loop [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 10, no. 3, pp. 9-15, Summer 2018, doi: 10.1109/MSSC.2018.2844615.

- Voltage Controlled Delay Line

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