3-BIT ANALOG TO DIGITAL CONVERTER IMPLEMENTED USING eSIM

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***Abstract* – The scope of this work is to present a 3-Bit Analog to Digital Converter. The main function of an ADC is to convert the input analog signal to digital signal. The building blocks of an flash type ADC mainly are Comparators and Encoders.**

***Keywords* – DIFFERENTIAL CURRENT STARVED VCO, LOW POWER CSVCO, PLL**

I. INTRODUCTION

Every signal found in the world is Analog in nature but the computers do no understand analog inputs; so to process the analog signals we have to convert it into 1's and 0's. Basically an ADC takes a snapshot of an analog voltage at one instant in time and produces a digital output code which represents this analogue voltage. The number of binary digits, or bits used to represent this analogue voltage value depends on the resolution of an A/D converter.
For example a 2-bit ADC will have a resolution of 3 whereas an 3-bit ADC will have a resolution of 7. Thus an ADC takes an unknown continuous analog signal and converts it into an n-bit binary number of 2 to the power n bits.

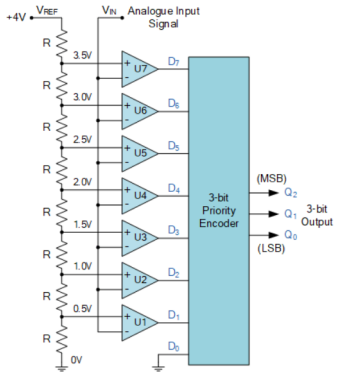

Fig. 1. Analog to Digital Converter Block Diagram

II. 8X3 Priority Encoder

An Encoder has a maximum of 2 to the power n input lines and 'n' output lines, hence it encodes the information from 2 to the power n inputs into an n-bit code. It will produce a binary code equivalent to the input, which is active High. An 8 to 3 priority encoder has 8 inputs : Y7, Y6, Y5, Y4, Y3, Y2, Y1 & Y0 and 3 outputs : A2, A1 & A0. Here, the input, Y7 has the highest priority, whereas the input, Y0 has the lowest priority.

III. Comparator Circuit

A comparator is a circuit that compares two voltages or currents and outputs a digital signal indicating which is larger.

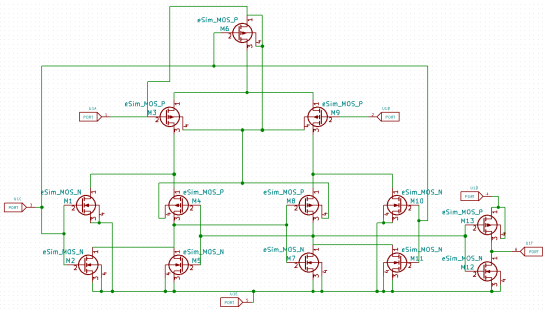

Fig. 2. Comparator Circuit

Coming to the working of this circuit, the Port 1 will be the Vref and Port 2 will be Vin and when Vin is higher than Vref the supply potential to the inverter set M8,M7 will be higher than the inverter set M4,M5, hence overpowering the ouput to give HIGH sinceM4,M5 will be in cutoff condition. Whereas in the inverted condition where the Vref is higher than Vin the inverter set M8,M7 will be in cutoff hence giving LOW as the ouput. When the Port 3 i.e Reset is high, the potential at ground i.e LOW is flooded to the supply of the inverter sets M8,M7 and M4,M5 giving output as LOW.

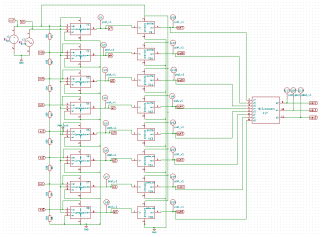

Fig. 3. 3-Bit ADC Schematic

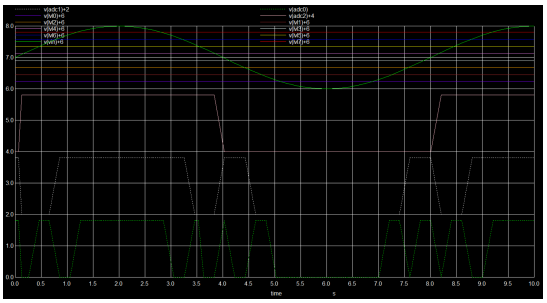

Fig. 4. 3-Bit ADC transient

References

1. www.electronics-tutorials.ws