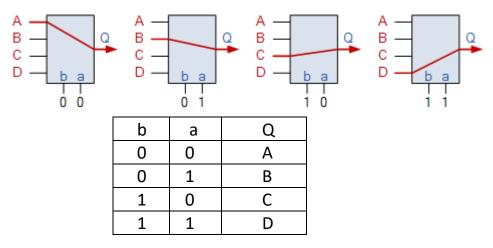
Title:- 74153 A Dual 4 line to 1 line Multiplexer

Theory :-

The multiplexer, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

The Function of a 4:1 Multiplexer with A,B,C,D as input lines and a,b as select inputs. Output Q is selected among A,B,C,D based on select inputs a,b.



Here 74153 is a dual 4 to 1 multiplexer with two select inputs (S1,S0) common to both the multiplexers.

a0,a1,a2,a3 are the inputs and Ya is the output , EA is the enable to the MUX1.

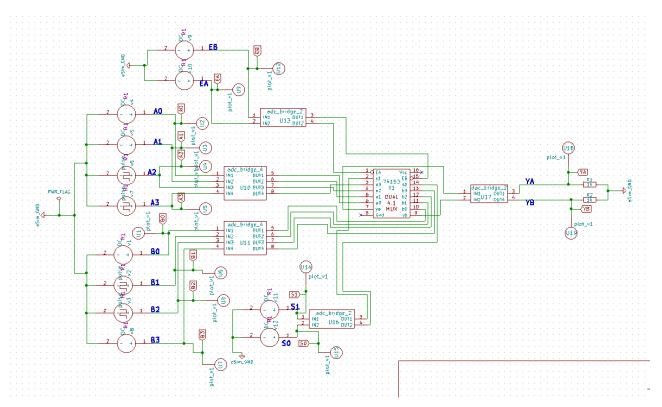
b0,b1,b2,b3 are the inputs and Yb is the output ,EB is the enable to the MUX2.

EA,EB	are activ	ve low en	able input	s.
	64	~~~	F A	

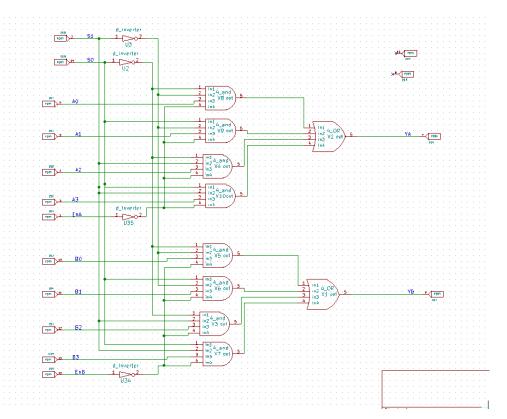
S1	SO	EA	Ya	EB	Yb
х	х	1	0	1	0
0	0	0	a0	0	b0
0	1	0	a1	0	b1
1	0	0	a2	0	b2
1	1	0	a3	0	b3

NOTE :- Here in E-SIM software, no need to connect Vcc(pin 16) and GND (pin 8) pins to Dc source and gnd respectively , you can leave them unconnected using NO CONNECT symbol . This is because in circuit simulation softwares , we use BASIC GATES (AND, NAND etc.) they don't need Vcc and GND. As in manufacturing an IC , they use MOSFETs to implement those GATES ,there MOSFETs require Vcc and Gnd

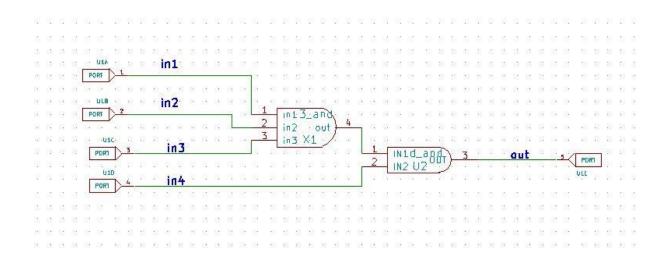
Schematic Diagram :-



Subcircuit Schematic for 74153 :



Subcircuit Schematic for "4_and" gate used in 74153 subcircuit :



Subcircuit Schematic for " 4_OR" gate used in 74153 subcircuit :

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	1 Tutat as	101 102 1	202 10208 302	20201-202	202 10202 10
	1N10_0607-	3	10.00 FORMA 3.00F	603009-0033	1002 000000 30
	IN2U2	1.5		Route and	
many and take many	not ported that had be	2	INU OBUT	001	
Fn: *			FIN2U4	1000103 (1001	· · · ·
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in4	(INZUS-7		2007 200902 2004	200703 2002	2014 2014016 20
reason and and reason	en resen ava sen re-	. 485 185	806 10.008 ASA	123631 3232	202 102031 40

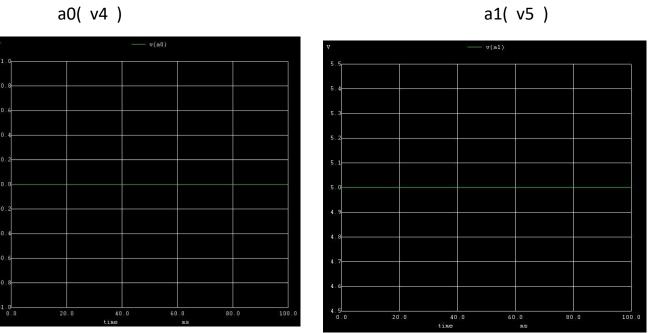
Subcircuit Schematic for " 3_and" gate used in 4_and gate :

Trons L in1	I INId_agg 3				
	IN2 U2 U2	INLd_0880) 3	tuo	4/[2007]	12
HE INT		IN2 U3 001		uLD .	
POR					
NO 1000 100 1000 100			80.0221.02	NOS NOSCI (NOS N	

Ngspice plots

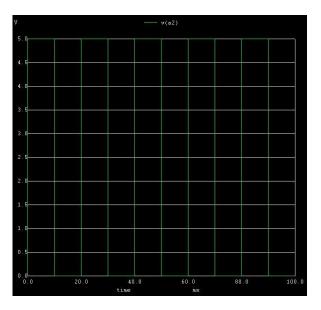
Inputs to MUX 1

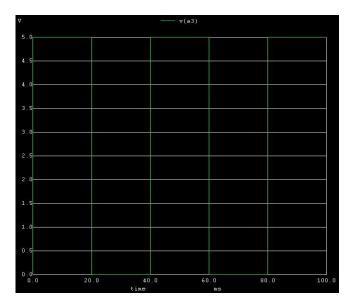




a2(v6)



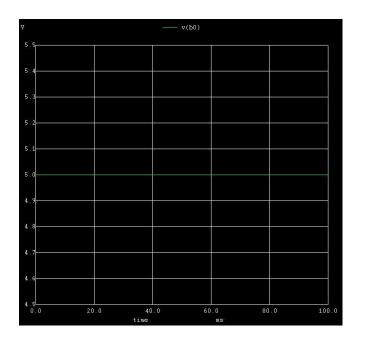


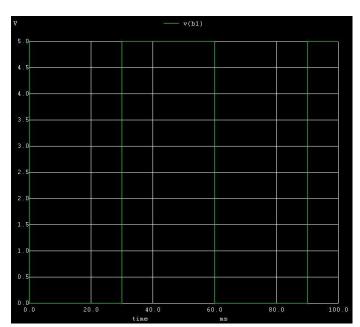


Inputs to MUX 2

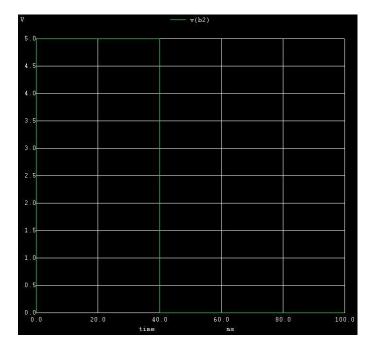
bO(v1)



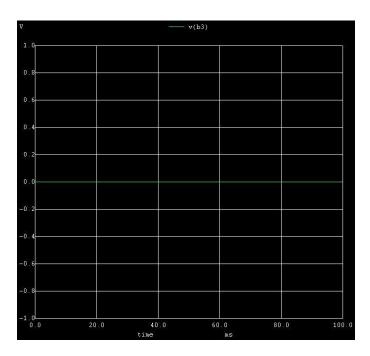




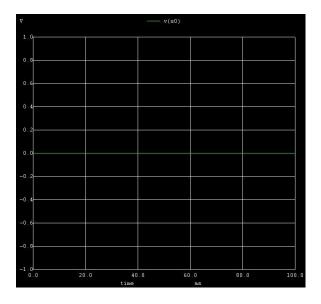
b2(v3)



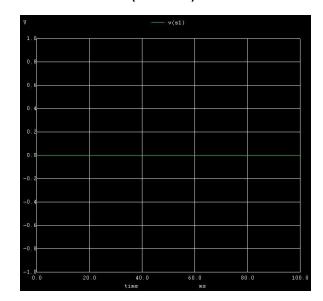




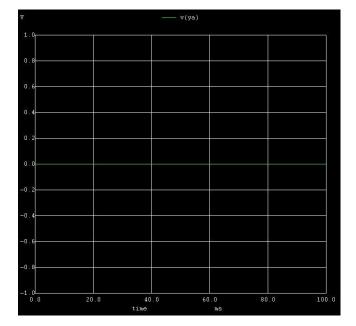
s0(v12=0v)



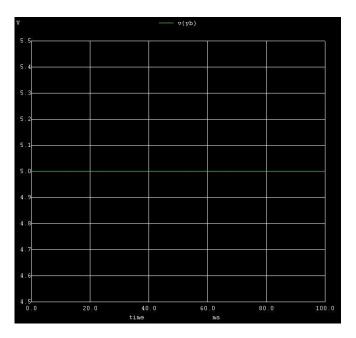
s1(v11=0v)



ya

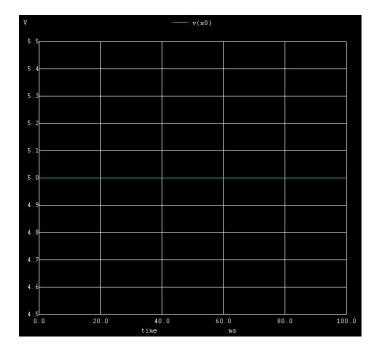




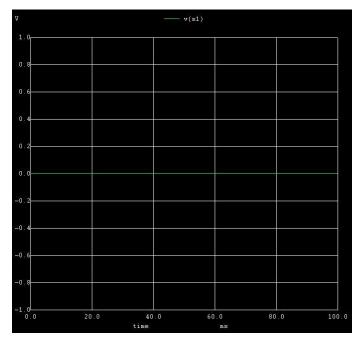


OUTPUTS when s0='1' and s1='0'

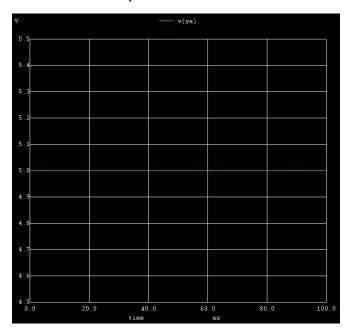
s0(v12=5v)

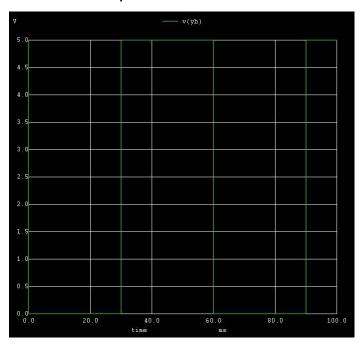


s1(v11=0v)



ya

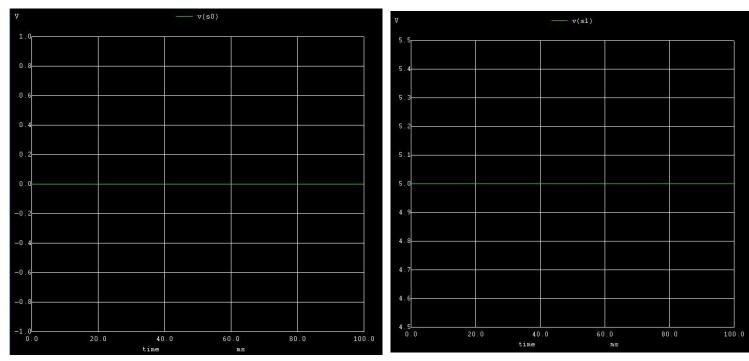




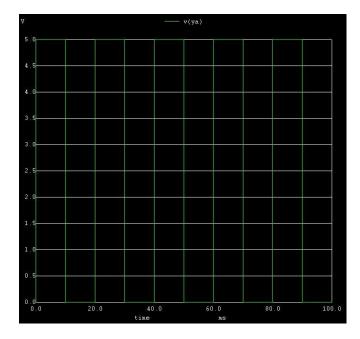
OUTPUTS when s0='0' and s1='1'

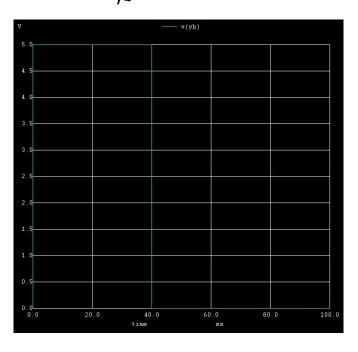






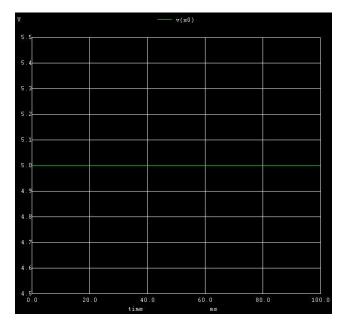
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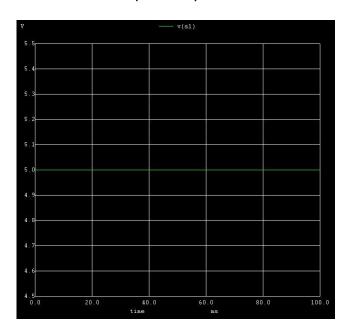


OUTPUTS when s0='1' and s1='1'

s0(v12=5v)

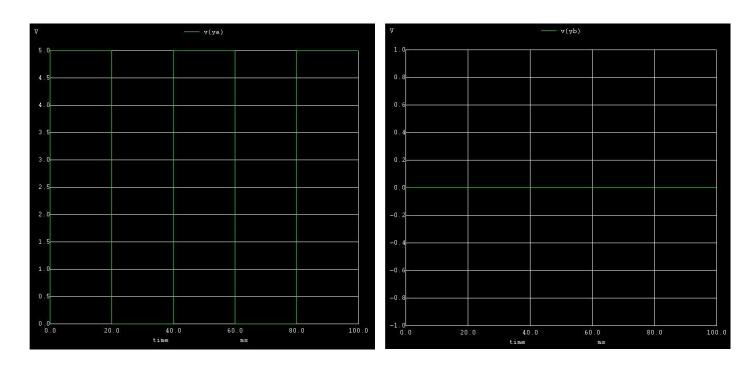


s1(v11=5v)



yb

ya

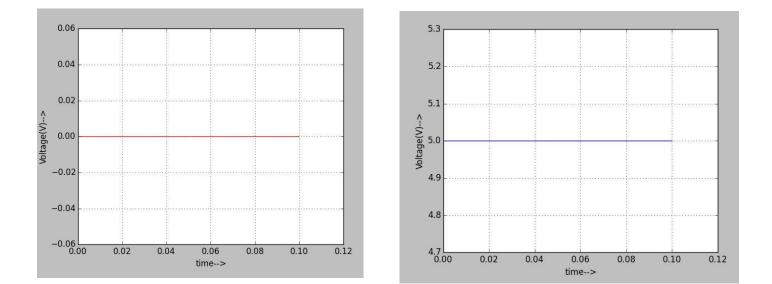


PYTHON PLOTS

Inputs to MUX 1

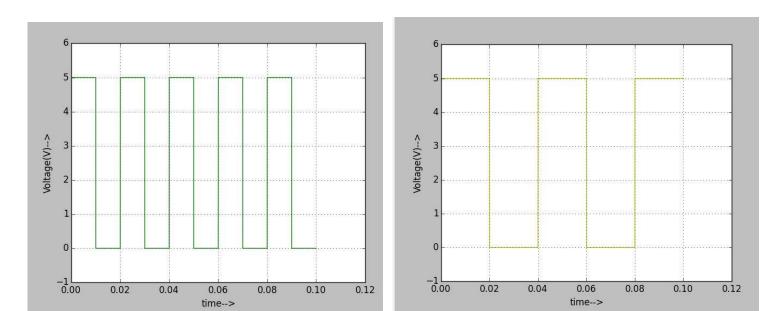
a0(v4)

a1(v5)



a2(v6)

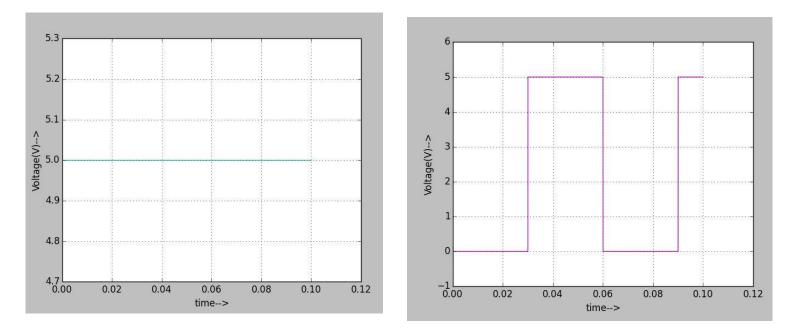




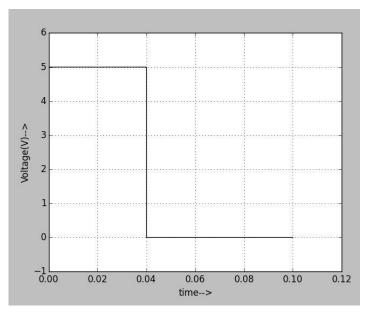
Inputs to MUX 2

bO(v1)

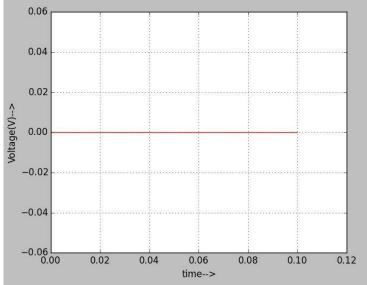
b1(v2)

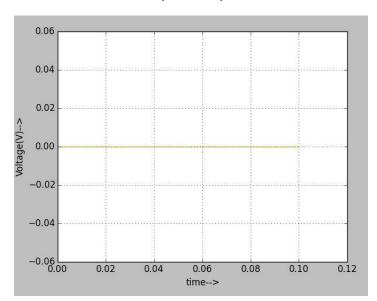


b2 (v3)

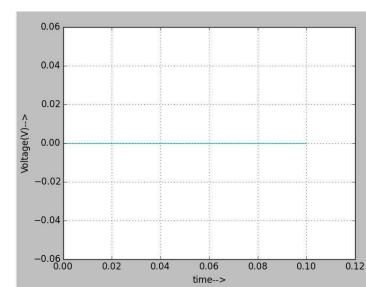


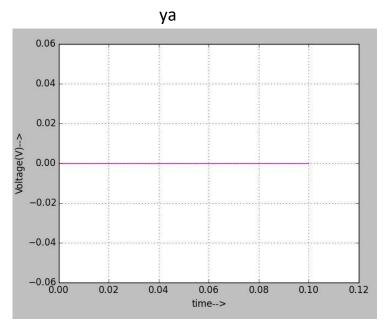
b3 (v8)



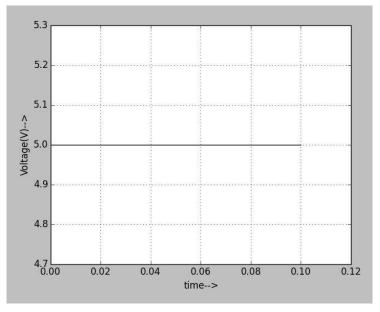


s0(v12=0v)





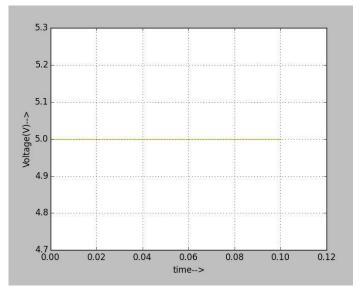
yb

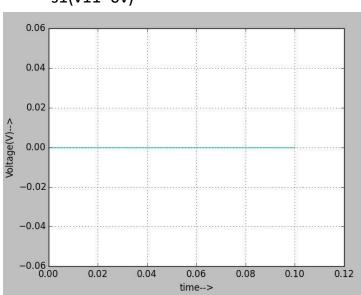


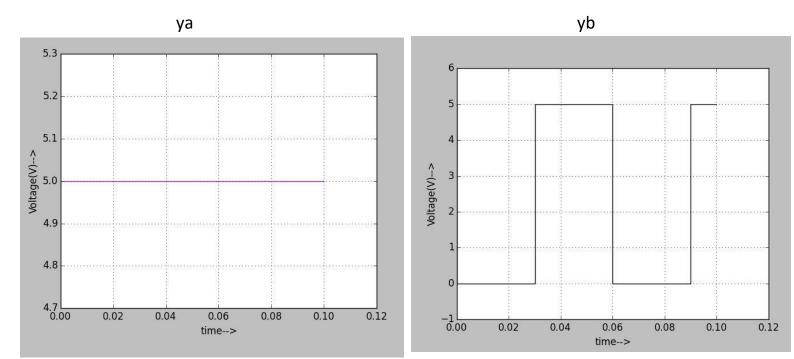
s1(v11=0v)

OUTPUTS when s0='0' and s1='1'



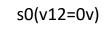




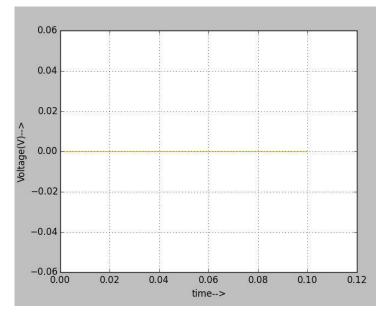


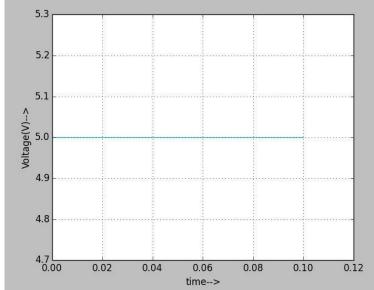
s1(v11=0v)

OUTPUTS when s0='0' and s1='1'

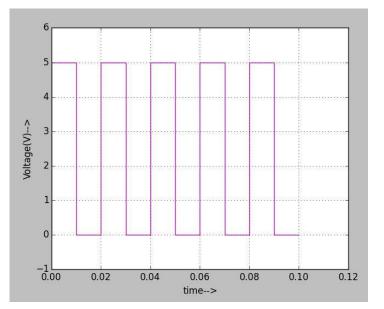


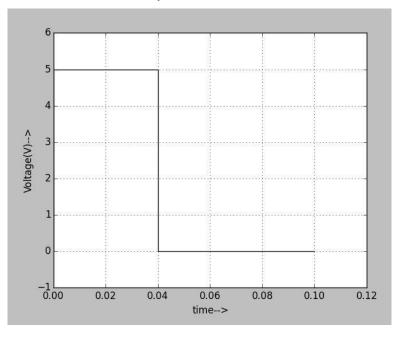


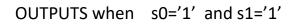




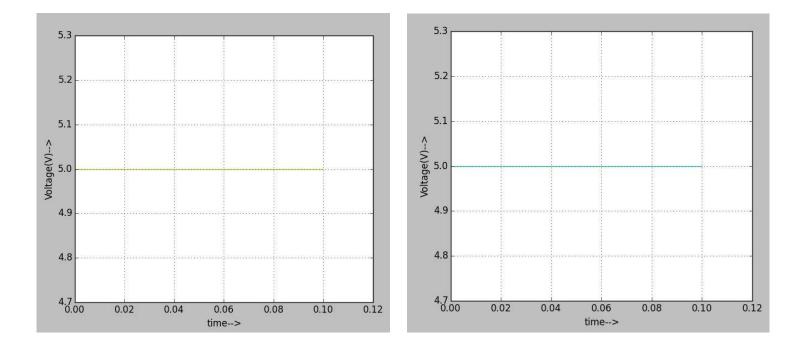
ya





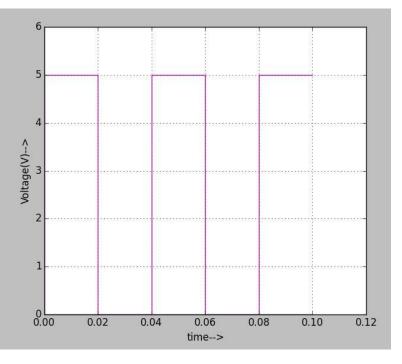


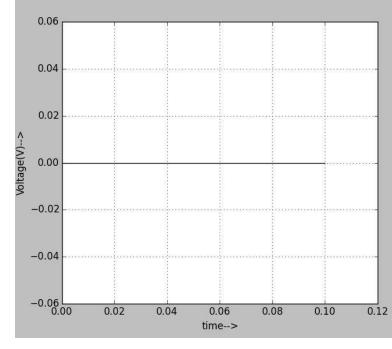
s0(v12=5v)



ya







REFERENCES:-

1) <u>https://www.electronicshub.org/multiplexerandmultiplexing/</u>

2)<u>https://www.ti.com/lit/ds/symlink/sn74ls153.pdf</u>